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EXAMINER	
KIM, DANIEL Y	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,446	BRIGGS ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement(s) received May 13, 2005 and January 12, 2004 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the Information Disclosure Statement(s) are being considered by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 5-6, 10-12, 15-16 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Murakami et al (US PGPub No. 20020120829; hereafter referred to as Murakami`829).

For claim 1, Murakami`829 discloses a memory control apparatus in a computing system (a data processor and a data processing system, par. 0001);

said memory controller and buffer being connected by a bidirectional data bus and a control interface (a bus controller that includes a plurality of instruction buffers, the bus controller further controls access to memory through a bus, par. 0032);

said buffer being connected to a random-access memory bus for read and write operations (whether an access request from a CPU is a request for data access, a request for instruction fetch, a read operation, or a write operation will be determined by having the memory access command on the memory access command bus decoded by a memory access command decoder and by sending the decoded result to an external memory access control unit, par. 0069; memory devices connectable may be selected from device types such as ROM, SRAM, DRAM, SDRAM, and others, par. 0066; fig. 8, items 17, 23, 30, 157-159);

said buffer comprising data storage areas to buffer data between the memory controller and system memory, said buffer further comprising logical circuits to decode memory interface control commands from said memory controller (par. 0069);

and a data access and control bus connected between the buffer and the system memory to control read and write operations from and to system memory (par. 0069).

For claim 5, Murakami`829 discloses the control interface between the memory controller and buffer comprises: a memory interface address bus for transferring memory addresses from the memory controller to the buffer (the address of the instruction to be supplied is output to an address bus of the memory, par. 0102; fig. 8, item 16).

For claim 6, Murakami`829 discloses the control interface between the controller and buffer comprises: a memory interface control bus for transferring memory control commands from the controller to the buffer (a memory access command generation unit outputs a memory access command onto a memory access command bus, par. 0063; fig.8, item 17).

For claim 10, Murakami`829 discloses the buffer comprises: control logic for decoding memory interface control commands (whether an access request from a CPU is a request for data access, a request for instruction fetch, a read operation, or a write operation will be determined by having the memory access command on the memory access command bus decoded by a memory access command decoder and by sending the decoded result to the external memory access control unit, par. 0069; fig. 8, item 23).

For claim 11, Murakami`829 discloses the buffer comprises: multiple data and control interfaces to system memory, one to interface with each independent portion of system memory (the external memory access control unit will supply the access control information such as chip selection signals to the memory device of the target for access to the external memory, and causes an address/data I/O control unit to control the supply of address signals as well as data input and output, par. 0070; fig. 8, items 4, 24, 200).

For claim 12, Murakami`829 discloses a method for data transfer between a memory controller and a system memory bus connected to system memory in a computing system comprising:

interposing a buffer between said system memory bus and the memory controller (fig. 8, items 157-159, 15-17, 20, 24);

providing to said buffer memory interface addresses and memory interface control commands to facilitate said buffer's read and write operations from and to said system memory (fig. 8, items 15-17, 22-23);

addressing said system memory through said buffer to accomplish read and write operations between the system memory and the memory controller (fig. 8, items 157-159, 15-17, 24);

decoding in said buffer the memory interface control commands (an instruction decoding facility to either the instruction buffer or buffer controller circuit, par. 0028);

temporarily storing data read and write memory data in the buffer during data transfer between the system memory and the buffer (this limitation is inherent of buffers); and

transferring read and write memory data between said memory controller and said buffer during read and write operations (fig. 8, items 20, 30, 157-159, 211).

For claim 15, Murakami`829 discloses controlling read and write operations to said system memory with the decoded memory interface control commands originating in the memory controller and decoded in the buffer (an instruction decoding facility to either the instruction buffer or buffer controller circuit to decode the instructions stating prefetch of instructions into the instruction buffer, par. 0028; a bus controller controls access to memory through a bus based on signals originating from the instruction

executing unit, par. 0032; the buffer control circuit may output instructions from the corresponding instruction buffer to the instruction executing unit, par. 0022).

For claim 16, Murakami`829 discloses fanning memory address information received in the buffer from the controller to the system memory through a data address control bus connecting the buffer to the system memory bus (fig. 8, items 16, 211, 30, 157-159, 20, 24, 200).

For claim 18, Murakami`829 discloses a memory control apparatus in a computing system comprising:

a memory controller and a means for buffering data between said controller and system memory (fig. 8, items 20, 24, 30, 157-159, 200);

said memory controller and buffer means being connected by a bidirectional data bus and a control interface (fig. 8, items 20, 24, 30, 157-159, 15-17);

said buffer means being connected to multiple random-access memory busses for read and write operations (whether an access request from a CPU is a request for data access, a request for instruction fetch, a read operation, or a write operation will be determined by having the memory access command on the memory access command bus decoded by a memory access command decoder and by sending the decoded result to an external memory access control unit, par. 0069; memory devices connectable may be selected from device types such as ROM, SRAM, DRAM, SDRAM, and others, par. 0066; fig. 8, items 17, 23, 30, 157-159);

said buffer means comprising means for temporarily storing data exchanged between the memory controller and system memory (the buffer controller stores entries

in the instruction buffers, par. 0075), said buffer means further comprising logical circuits to decode memory interface control commands from said memory controller (fig. 8, items 22-23); and

a data access and control bus connected between the buffer and the multiple random-access memory busses to control read and write operations from and to system memory (fig. 8, items 15-17, 200).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-4 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al (US PGPub No. 20020120829; hereafter referred to as Murakami`829) and Murakami et al (US Patent No. 6,839,806; hereafter referred to as Murakami`806).

For claim 2, Murakami`829 discloses the invention as per rejection of claim 1 above. These teachings do not, however, disclose any of the limitations of claim 2.

Murakami`806, however, discloses a second buffer serving as a tag buffer, said second buffer being connected to said random-access memory bus for read and write operations (a cache tag buffer, cache tag memory and cache control circuit, col. 2, lines

23-34; a memory bus interface for connecting the shared bus to the cache system, col. 3, lines 10-11);

said second buffer comprising data storage areas to buffer data between the memory controller and system memory, said buffer further comprising logical circuits to decode memory interface control commands from said memory controller (when a read transaction or a write transaction to main memory is issued from a processor, the cache system receives the transaction in the processor interface via a bus, col. 4, lines 18-44; fig. 1, items 210, 280, 30); and

a data access and control bus connected between the tag buffer and the system memory to control read and write operations from and to system memory (a memory bus interface for connecting the shared bus to the cache system, col. 3, lines 10-11; fig. 1, items 30, 220, 20).

Murakami`829 and Murakami`806 are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a tag buffer, decoding interface and bus in the present invention because by providing a cache tag buffer system for storing part of a cache tag memory, it is possible to reduce the number of times access is made to the cache tag memory, thereby reducing the cache access latency in a system (col. 2, lines 54-57), as taught by Murakami`829.

For claim 3, Murakami`829 discloses a tag control input signal designating a second buffer (a plurality of instruction buffers, and a flag intrinsic to each of the instruction buffers, and a buffer control circuit, and that the buffer control circuit may

allocate to each of the instruction buffers one of intrinsic values, par. 0016). Murakami`806 then further discloses providing a cache tag buffer (col. 2, lines 54-55).

For claim 4, Murakami`829 discloses the invention as per rejection of claim 3 above. Murakami`806 further discloses a memory interface tag bus between the memory controller and second buffer (a cache control circuit reads out the content of a cache tag buffer via a path, and writes tags and states of cache blocks corresponding to the tags into the ache buffer via another path, col. 4, lines 27-40).

Claim 13 is rejected using the same rationale as for the rejection of claims 2 and 12 above.

For claim 14, Murakami`829 discloses the invention as per rejection of claim 12 above. These teachings do not, however, disclose updating memory tag information through a tag interface control bus between the memory controller and the tag buffer.

Murakami`806, however, discloses when a read or write transaction to main memory is issued from a processor, the cache system receives the transaction in the processor interface via a bus, and a cache control circuit writes all index addresses of a set of cache tag memory and all the tags in the set as well as all the states of the cache blocks corresponding to the tags into a cache tag buffer via a path (col. 4, lines 18-44; fig. 1, items 270, 280, 506).

Murakami`829 and Murakami`806 are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a tag interface control bus between the memory controller and tag buffer because this

would connect devices and allow for the receiving of transactions through a path (col. 4, lines 20-23), as taught by Murakami`806.

6. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al (US PGPub No. 20020120829; hereafter referred to as Murakami`829) and Sah et al (US PGPub No. 20030177320).

For claim 7, Murakami`829 discloses the invention as per rejection of claim 1 above. These teachings do not, however, disclose a buffer comprises: a read data queue.

Sah, however, discloses a memory read queue and a pending data buffer (par. 0177).

Murakami`829 and Sah are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a read data queue because this would allow for the holding of multiple read requests, and because by examining the contents of the queues, the order in which read and write requests are presented to memory may be changed to avoid or minimize conflicts that could otherwise impair the efficiency of memory operations (abstract).

For claim 8, Murakami`829 discloses the invention as per rejection of claim 1 above. These teachings do not, however, disclose a buffer comprises: a write data queue.

Sah, however, discloses a memory write queue and a pending data buffer (par. 0177).

Murakami`829 and Sah are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a write data queue because this would allow for the holding of multiple write requests, and because by examining the contents of the queues, the order in which read and write requests are presented to memory may be changed to avoid or minimize conflicts that could otherwise impair the efficiency of memory operations (abstract).

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al (US PGPub No. 20020120829; hereafter referred to as Murakami`829) and McClannahan et al (US PGPub No. 20040117566).

For claim 9, Murakami`829 discloses the invention as per rejection of claim 1 above. These teachings do not, however, disclose a buffer comprises: a tag data queue.

McClannahan, however, discloses an inbound tag queue (par. 0073).

Murakami`829 and McClannahan are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a tag data queue because this would allow for the ordering of links between a requesting entity and an operation (par. 0070), and because an operation that does not

return data need only send a tag to the requester to indicate an error has occurred (par. 0070), as taught by McClannahan.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al (US PGPub No. 20020120829; hereafter referred to as Murakami`829) and Prasad (US PGPub No. 20030163776).

For claim 17, Murakami`829 discloses the invention as per rejection of claim 12 above. These teachings do not, however, disclose interleaving read and write operations in sequences of memory operations between a controller and multiple independent portions of system memory through a buffer.

Prasad, however, discloses a single memory buffer is used for interleaving by alternating read and write operations (par. 0067).

Murakami`829 and Prasad are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include interleaving operations because this would improve error performance in that a decoder could handle errors more readily (par. 0004), as taught by Prasad.

Citation of Pertinent Prior Art

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dugan et al (US PGPub No. 20010034815) discloses a memory controller for read and write requests and tag buffer units for updating tags associated with memory lines and transferring data between the controller and a main memory.

Hann et al (US Patent No. 6,853,643) discloses a memory controller maintains a read queue to store read requests from a scheduler and a write queue to store write requests from an enqueuer.

Shibayama (US Patent No. 6,678,789) discloses a memory system with a storage buffer, cache memory, and tag buffer.

Walker et al (US Patent No. 6,874,116) discloses memory system including both a tag buffer and data buffer.

Contact Information

10. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions

regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

3-31-06

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